AMENDMENTS TO THE CLAIMS

Please amend the claims as follows:

Listing of Claims:

Claim 1 (Currently Amended): Stereo demultiplexer configured ~~and adapted for receiving~~ to receive a frequency demodulated stereo-multiplex signal ~~(m(t))~~ which comprises at least a stereo-difference signal ~~(m$_d$(t))~~, a stereo-sum signal ~~(m$_s$(t))~~ and a pilot carrier, said stereo demulitplexer comprising:

a decimation filter configured to extract, from said frequency demodulated stereo-multiplex signal, a sampling rate decimated signal decimated by a factor D regarding said frequency demodulated stereo-multiplex signal, thereby providing the stereo-sum signal and the pilot carrier signal and eliminating the stereo-difference signal; and

a PLL-circuit configured ~~and adapted~~ to receive said extracted signal as an input signal and for recovering, from said input signal, the pilot carrier or at least one harmonic ~~thereof~~ of the pilot carrier to perform an amplitude demodulation, ~~wherein said PLL-circuit receives an input signal that, in essence, solely comprises said stereo-sum signal (m$_s$(t)) and said pilot carrier, wherein said input signal is sampling rate decimated by a decimation factor of D with regard to said received frequency demodulated stereo-multiplex signal~~.

Claim 2 (Currently Amended): Stereo demultiplexer according to claim 1, ~~wherein said sampling rate decimated stereo-sum signal (m$_s$(t)) is further sampling rate decimated by a decimation factor of E before said PLL-circuit receives it as input signal~~ further comprising:

sampling rate decimation means configured to further decimate the sampling rate of said extracted signal by a decimation factor E, before said PLL-circuit receives the signal that passed through the decimation filter and the sampling rate decimation means.

Claim 3 (Currently Amended): Stereo demultiplexer <u>according to claim 1</u> ~~configured and adapted for receiving a frequency-demodulated stereo-multiplex signal (m(t)) which comprises at least a stereo-difference signal (m~~$_d$~~(t)), a stereo-sum signal (m~~$_s$~~(t)) and a pilot carrier, comprising a PLL-circuit configured and adapted for recovering the pilot carrier or at least one harmonic thereof to perform an amplitude demodulation, wherein said PLL-circuit receives an input signal that, in essence, solely comprises said stereo-sum signal (m~~$_s$~~(t)) and said pilot carrier, wherein said input signal is sampling rate decimated by a decimation factor of D with regard to said received frequency-demodulated stereo-multiplex signal,~~

wherein said PLL-circuit ~~outputs~~ <u>is configured to output</u> a recovered pilot carrier which is interpolated so that ~~it~~ <u>the recovered pilot carrier</u> has a sampling rate equal to that of the frequency demodulated stereo-multiplex signal.

Claim 4 (Currently Amended): Stereo demultiplexer according to claim 3, wherein ~~that~~ <u>said PLL-circuit comprises:</u>

<u>means configured to alternately output</u> D-1 or (E·D)-1 interpolated pilot carrier values (y(k/D+1), ..., y(k/D+(D-1))) and one calculated pilot carrier value (y(k/D)) ~~are alternately output~~.

Claim 5 (Currently Amended): Stereo demultiplexer according to claim 4, wherein <u>said PLL-circuit is further configured to perform</u> said interpolation ~~within the PLL-circuit is performed~~ on <u>a</u> basis of a prediction starting at said calculated pilot carrier value.

Claim 6 (Currently Amended): Stereo demultiplexer according to claim 5, <u>further</u> including<u>:</u>

[[-]] a PLL within the PLL-circuit <u>configured to output</u> ~~which outputs~~ a phase signal, and

[[-]] a first sine calculation unit <u>configured to output</u> ~~which outputs~~ said one calculated pilot carrier value (y(k/D)) on ~~the~~ <u>a</u> basis of said phase signal.

Claim 7 (Currently Amended): Stereo demultiplexer according to claim 6, <u>further</u> including<u>:</u>

[[-]] second to Dth or (E·D)th sine calculation units each <u>configured to output</u> ~~of which outputs~~ one of said D-1 or (E·D)-1 interpolated pilot carrier values (y(k/D+1), ..., y(k/D+(D-1))) on <u>a</u> basis of said phase signal and a respective added phase shift value.

Claim 8 (Currently Amended): Stereo demultiplexer according to claim 6, <u>further</u> including<u>:</u>

[[-]] a third multiplexer <u>configured to multiplex</u> ~~which multiplies~~ said phase signal with a factor ~~of~~ 2 before <u>the phase signal</u> ~~it~~ is input to said first sine calculation unit or a respective second to Dth or (E·D)th sine calculation unit via a respective second to Dth or (E·D)th adder<u>, configured to add</u> ~~which adds~~ said respective phase shift value so that the 2nd harmonic of the pilot carrier is generated.

Claim 9 (Currently Amended): Stereo demultiplexer according to claim 6, wherein said PLL comprises<u>:</u>

[[-]] a first multiplier <u>configured to receive</u> ~~receiving~~ samples of the stereo-sum signal ~~(x(k))~~ as multiplicant at a first input,

[[-]] a filter ~~receiving~~ <u>configured to receive</u> the output signal of said first multiplier,

[[-]] a second multiplier ~~multiplying~~ <u>configured to multiply</u> said output signal of said filter with a PLL gain ~~(PLL loop gain)~~,

[[-]] a first adder ~~receiving~~ <u>configured to receive</u> said output signal of said second multiplier at a first input as a first summand, <u>configured to receive</u> a constant representing the product of ~~the~~ <u>a</u> pilot carrier frequency ~~(ω_{pil})~~ and the sampling period at a second input as a second summand, and <u>configured to receive</u> a delayed phase signal which is the output signal of said first adder at a third input as a third summand,

[[-]] a delay element ~~receiving~~ <u>configured to receive</u> said phase signal of said first adder and <u>configured to supply</u> ~~supplying~~ said delayed phase signal to said third input of said first adder, and

[[-]] a cosine calculation unit ~~receiving~~ <u>configured to receive</u> the phase signal of said first adder and <u>configured to supply</u> ~~supplying its~~ <u>an</u> output signal <u>of the cosine calculation unit</u> as multiplier to a second input of said first multiplier.

Claims 10-19 (Canceled).

Claim 20 (Currently Amended): Stereo demultiplexer according to claim 6, including

[[-]] a third multiplexer <u>configured to multiply</u> ~~which multiplies~~ said phase signal with a factor ~~of~~ 2 before <u>the phase signal</u> ~~it~~ is input to said first sine calculation unit and a respective second to D^{th} or $(E \cdot D)^{th}$ sine calculation unit via a respective second to D^{th} or $(E \cdot D)^{th}$ adder ~~which adds~~ <u>configured to add</u> said respective phase shift value so that the 2nd harmonic of the pilot carrier is generated.

Claim 21 (Currently Amended): The stereo demultiplexer of claim 1, <u>further</u> comprising:

channel recovery means configured <u>to recover</u> ~~and adapted for recovering~~ a left or right channel associated with said stereo-multiplex signal on <u>a</u> ~~the~~ basis of first and second intermediate signals; and

a sampling rate decimator configured <u>to decimate a</u> ~~and adapted for~~ sampling rate ~~decimating~~ <u>of</u> one of said first and second intermediate signals by a decimation factor E, and ~~supplying~~ <u>configured to supply</u> said sampling rate decimated intermediate signal to said PLL-circuit as said input signal.

Claim 22 (Currently Amended): The stereo demultiplexer of claim 21, wherein said channel recovery means is an adder configured <u>to receive</u> ~~and adapted for receiving~~ said first and second intermediate signals as an input.

Claim 23 (Currently Amended): The stereo demultiplexer of claim 1, <u>further</u> comprising:

channel recovery means configured <u>to recover</u> ~~and adapted for recovering~~ a left or right channel associated with said stereo-multiplex signal on the basis of first and second intermediate signals,

wherein said input signal is one of said first and second intermediate signals.

Claim 24 (Currently Amended): The stereo demultiplexer of claim 23, wherein said channel recovery means is an adder configured <u>to receive</u> ~~and adapted for receiving~~ said first and second intermediate signals as an input.

Claim 25 (Currently Amended): The stereo demultiplexer of claim 1, wherein said PLL-circuit <u>is configured to output</u> ~~outputs~~ a recovered pilot carrier which is interpolated so

that it the recovered pilot carrier has a sampling rate equal to that of the frequency

demodulated stereo-multiplex signal.